What is claimed is:

1. A semiconductor memory device comprising:

a memory-cell array comprising a plurality of memory cells laid out therein as memory cells each capable of storing data;

a read circuit used in a data read operation to read out data from said memory-cell array;

a write circuit used in a data write operation to write data into said memory-cell array;

a read clock generation circuit for generating a read clock signal to be supplied to said read circuit in said data read operation to read out data from said memory-cell array;

a write clock generation circuit for generating a write clock signal to be supplied to said write circuit in said data write operation to write data into said memory-cell array;

a read pulse-width adjustment circuit provided in said read clock generation circuit for adjusting the pulse width of said read clock signal generated by said read clock generation circuit; and

a write pulse-width adjustment circuit provided in said write clock generation circuit for adjusting the pulse width of said write clock signal generated by said write clock generation circuit, wherein said pulse width of said

read clock signal and said pulse width of said write clock signal are adjusted individually.

2. A semiconductor memory device according to claim 1 wherein:

said read circuit or said write circuit has a plurality of ports with any one of said ports allowing data to be read out from said memory-cell array or written into said memory-cell array in a manner independent of the other ports; and

said read pulse-width adjustment circuit or said write pulse-width adjustment circuit is provided for each of said ports.

3. A semiconductor memory device according to claim 1 wherein:

said read pulse-width adjustment circuit and said write pulse-width adjustment circuit each have a delay circuit and a delay adjustment circuit for adjusting a signal delay of said delay circuit; and

said delay adjustment circuit includes a fuse circuit for determining a state of a control signal for adjusting said signal delay of said delay circuit.

4. A semiconductor memory device according to claim 1 wherein:

said read pulse-width adjustment circuit and said write pulse-width adjustment circuit each have a delay circuit and a delay adjustment circuit for adjusting a

signal delay of a delay circuit; and

said delay adjustment circuit includes a flip-flop circuit for determining a state of a control signal for adjusting said signal delay of said delay circuit.

5. A semiconductor memory device comprising:

a memory-cell array comprising a plurality of memory cells laid out therein as memory cells each capable of storing data;

a read circuit used in a data read operation to read out data from said memory-cell array;

a write circuit used in a data write operation to write data into said memory-cell array;

a read clock generation circuit for generating a read clock signal to be supplied to said read circuit in said data read operation to read out data from said memory-cell array;

a write clock generation circuit for generating a write clock signal to be supplied to said write circuit in said data write operation to write data into said memory-cell array;

a read pulse-width adjustment circuit provided in said read clock generation circuit as a circuit for adjusting the pulse width of said read clock signal generated by said read clock generation circuit; and

a write pulse-width adjustment circuit provided in said write clock generation circuit as a circuit for

adjusting the pulse width of said write clock signal generated by said write clock generation circuit;

wherein:

said pulse width of said read clock signal and said pulse width of said write clock signal are adjusted individually;

said read pulse-width adjustment circuit provided in said read clock generation circuit has a delay circuit for delaying an input signal and a logic gate for forming a waveform on the basis of a signal output by said delay circuit; and

a plurality of said logic gates is provided at locations spread in said read circuit.

6. A semiconductor memory device according to claim 5 wherein:

said read circuit includes:

an address buffer for storing an address signal;

a row-system decode circuit for generating a selection signal, which is used for selecting a row system, on the basis of said address signal stored in said address buffer; and

a column-system decode circuit for generating a selection signal, which is used for selecting a column system, on the basis of said address signal stored in said address buffer;

one of said logic gates is provided for said row-system decode circuit included in said read circuit; and

another one of said logic gates is provided for said column-system decode circuit included in said read circuit.

7. A semiconductor memory device according to claim 6 wherein:

said logic gate provided for said row-system decode circuit outputs a signal representing computed logic of a signal generated by said row-system decode circuit and a signal generated by said delay circuit; and

said logic gate provided for said column-system decode circuit outputs a signal representing computed logic of a signal generated by said column-system decode circuit and a signal generated by said delay circuit.

8. A semiconductor memory device according to claim 5 wherein:

said read pulse-width adjustment circuit and said write pulse-width adjustment circuit each have a delay circuit and a delay adjustment circuit for adjusting a signal delay of said delay circuit; and

said delay adjustment circuit includes a fuse circuit for determining a state of a control signal for adjusting said signal delay of said delay circuit.

9. A semiconductor memory device according to claim 5 wherein:

said read pulse-width adjustment circuit and said

write pulse-width adjustment circuit a delay circuit and a delay adjustment circuit for adjusting a signal delay of said delay circuit; and

said delay adjustment circuit includes a flip-flop circuit for determining a state of a control signal for adjusting said signal delay of said delay circuit.

10. A semiconductor memory device comprising:

a memory-cell array comprising a plurality of memory cells laid out therein as memory cells each capable of storing data;

a read circuit used in a data read operation to read out data from said memory-cell array;

a write circuit used in a data write operation to write data into said memory-cell array;

a read clock generation circuit for generating a read clock signal to be supplied to said read circuit in said data read operation to read out data from said memory-cell array;

a write clock generation circuit for generating a write clock signal to be supplied to said write circuit in said data write operation to write data into said memory-cell array;

a read pulse-width adjustment circuit provided in said read clock generation circuit as a circuit for adjusting the pulse width of said read clock signal generated by said read clock generation circuit; and

a write pulse-width adjustment circuit provided in said write clock generation circuit as a circuit for adjusting the pulse width of said write clock signal generated by said write clock generation circuit;

wherein:

said pulse width of said read clock signal and said pulse width of said write clock signal are adjusted individually;

said read pulse-width adjustment circuit provided in said read clock generation circuit has a delay circuit for delaying an input signal and a logic gate for forming a waveform on the basis of a signal output by said delay circuit; and

a plurality of said logic gates is provided at locations spread in said write circuit.

11. A semiconductor memory device according to claim 10 wherein:

said write circuit includes:

an address buffer for storing an address signal;

a row-system decode circuit for generating a selection signal, which is used for selecting a row system, on the basis of said address signal stored in said address buffer; and

a column-system decode circuit for generating a selection signal, which is used for selecting a column

system, on the basis of said address signal stored in said address buffer;

one of said logic gates is provided for said row-system decode circuit included in said write circuit; and

another one of said logic gates is provided for said column-system decode circuit included in said write circuit.

12. A semiconductor memory device according to claim 11 wherein:

said logic gate provided for said row-system decode circuit outputs a signal representing computed logic of a signal generated by said row-system decode circuit and a signal generated by said delay circuit; and

said logic gate provided for said column-system decode circuit outputs a signal representing computed logic of a signal generated by said column-system decode circuit and a signal generated by said delay circuit.

13. A semiconductor memory device according to claim 10 wherein:

said read pulse-width adjustment circuit and said write pulse-width adjustment circuit each have a delay circuit and a delay adjustment circuit for adjusting a signal delay of said delay circuit; and

said delay adjustment circuit includes a fuse circuit for determining a state of a control signal for adjusting said signal delay of said delay circuit.

14. A semiconductor memory device according to claim

10 wherein:

said read pulse-width adjustment circuit and said write pulse-width adjustment circuit each have a delay circuit and a delay adjustment circuit for adjusting a signal delay of said delay circuit; and

said delay adjustment circuit includes a flip-flop circuit for determining a state of a control signal for adjusting said signal delay of said delay circuit.